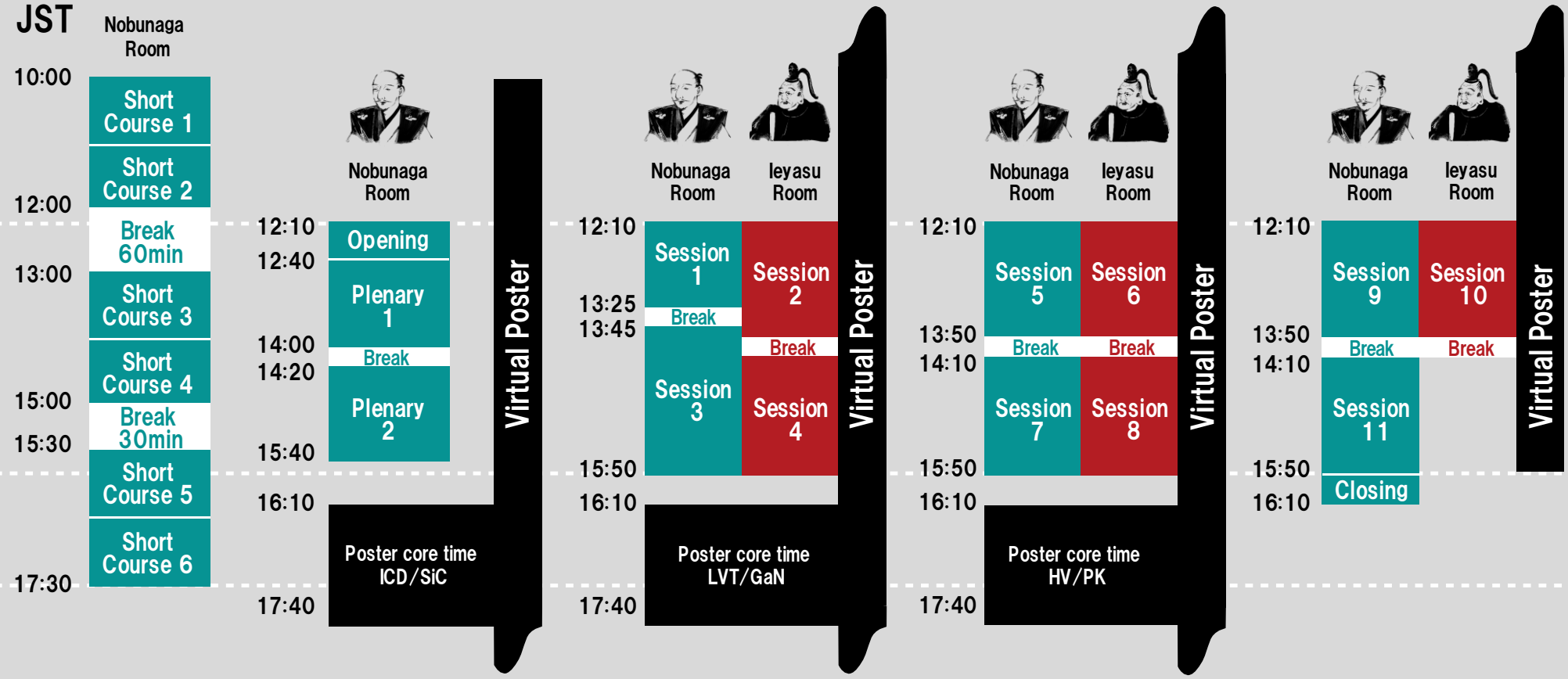
ISPSD2021 Virtual Rooms and Schedule



ISPSD2021 Session Layout

May 31,Mon

Nobunaga Room

12:10 – 12:40 **Opening**

12:40 – 14:00 **Plenary 1**

14:20 – 15:40 **Plenary 2**

June 1,Tue

Nobunaga Room

12:10 – 13:25 **Session 1**
(HV)
IGBTs

13:45 – 15:50 **Session 3**
(ICD)
ICs for High Efficiency & High Reliability

Ieyasu Room

12:10 – 13:50 **Session 2**
(GaN)
Dynamic Ron & Reliability of p-GaN Gate Technologies

14:10 – 15:50 **Session 4**
(SiC)
SiC Advanced Novel Devices

June 2,Wed

Nobunaga Room

12:10 – 13:50 **Session 5**
(LVT)
Lateral Low Voltage Devices

14:10 – 15:50 **Session 7**
(PK)
Packaging Technologies: Integrated Modeling & Design

Ieyasu Room

12:10 – 13:50 **Session 6**
(SiC)
SiC Device Ruggedness & Reliability

14:10 – 15:50 **Session 8**
(GaN)
Advances on Fin-FETs & Alternative p-typ Materials for GaN Devices

June 3,Thu

Nobunaga Room

12:10 – 13:50 **Session 9**
(HV/LVT)
Simulation Analysis for Silicon Vertical Devices

14:10 – 15:50 **Session 11**
(LVT)
Vertical Low Voltage Devices and Late News

15:50 – 16:10 **Closing**

Ieyasu Room

12:10 – 13:50 **Session 10**
(PK)
Packaging Technologies: Characterization & Reliability

Virtual Poster Sessions, 10:00 May 31- 15:50 June 3

Poster core time 16:10 ~ 17:40, May 31

Session P1
(ICD)
IC Design

Session P2
(SiC)
SiC Devices and Technology

Poster core time 16:10 ~ 17:40, June 1

Session P3
(LVT)
Low Voltage Devices and Power IC Device Technology

Session P4
(GaN)
GaN Devices and Technology

Poster core time 16:10 ~ 17:40, June 2

Session P5
(HV)
High Voltage Devices

Session P6
(PK)
Module and Package Technologies